

PATENT

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| Applicant: | Cheisan J. Yue and James D. Seefeldt | Confirmation No. | 1964 |
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| Examiner: | Amar Movva | | |
| Group Art Unit: | 2894 | | |
| Docket No.: | H0005049 | | |
| Title: | TECHNIQUES TO REDUCE SUBSTRATE CROSS TALK ON MIXED SIGNAL AND RF CIRCUIT DESIGN | | |

CERTIFICATE UNDER 37 CFR 1.8 I hereby certify that this correspondence is being transmitted via the United States Patent and Trademark Office electronic filing system on May 4, 2010.

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

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Sir:

Applicant respectfully requests a Pre-Appeal Brief Review based upon the Examiner's failure to establish a prima facie case of obviousness of claims 1-19, 40, and 41 under 35 U.S.C. § 103(a) in the Final Office Action dated February 4, 2010. As outlined below, the applied references fail to disclose or suggest one or more elements recited in Applicant's independent claim 1. For at least this reason, the rejection under 35 U.S.C. § 103(a) was improper.

For the sake of clarity, Applicant only presents arguments below with respect to claim 1. By setting forth the following clear grounds of error with respect to claim 1, Applicant does not assert that they are the only errors in the Final Office Action; nor does Applicant waive any additional arguments that may be asserted later in an Appeal Brief.

Independent Claim 1

Claim 1 requires an integrated circuit comprising: a semiconductor substrate, a buried insulation layer directly over the semiconductor substrate, a first semiconductor mesa over the buried insulation layer, a first guard ring substantially surrounding the first semiconductor mesa, wherein the first guard ring extends through the buried insulation layer contacting the semiconductor substrate, and wherein the first guard ring is arranged to provide RF isolation for the first semiconductor mesa, a second guard ring substantially surrounding the second semiconductor mesa, wherein the second guard ring extends through the buried insulation layer contacting the semiconductor substrate, and wherein the second guard ring is arranged to provide RF isolation for the second semiconductor mesa, and a third guard ring between the first and second guard rings, wherein the third guard ring is in contact with the semiconductor substrate, and wherein the third guard ring is arranged to provide further RF isolation for the first and second semiconductor mesas.

In support of the rejection under 35 U.S.C. § 103(a) of independent claim 1 in the Final Office Action, the Examiner indicated that claim 1 was unpatentable over U.S. Patent No. over Hiramoto (US 5,661,329) in view of Hutter (US 4,819,052). Applicant respectfully disagrees.

The Hiramoto and Hutter references fail to disclose or suggest all of the features of claim 1. The cited references, taken alone or in combination, fail to disclose or suggest, among other things, an integrated circuit that includes “a first guard ring substantially surrounding [a] first semiconductor mesa, wherein the first guard ring extends through [a] buried insulation layer contacting the semiconductor substrate, and wherein the first guard ring is arranged to provide RF isolation for the first semiconductor mesa.” The cited references, taken alone or in combination, also fail to disclose or suggest “a second guard ring substantially surrounding [a] second semiconductor mesa, wherein the second guard ring extends through the buried insulation layer contacting the semiconductor substrate, and wherein the second guard ring is arranged to provide RF isolation for the second semiconductor mesa.”

Applicant respectfully submits that the Examiner failed to identify features in Hiramoto and Hutter that correspond to all of the elements of claim 1. Moreover, the Examiner did not point to any apparent reason to modify the Hiramoto device in view of Hutter to include such elements, as is necessary to support a prima facie case of obviousness. In particular, the Examiner failed to identify any feature in Hiramoto or Hutter that corresponds to a first or

second guard ring that “extends through [a] buried insulation layer contacting the semiconductor substrate,” as required by claim 1. It is clear that “obviousness requires a suggestion of all limitations in a claim.” *CFMT, Inc. v. Yieldup Intern. Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003) (citing *In re Royka*, 490 F.2d 981, 985 (CCPA 1974)). To the extent that any limitation is missing from the prior art, such that modification would be necessary to incorporate such a limitation, the Examiner must demonstrate the obviousness of such a modification. In so doing, the Examiner must provide “*some articulated reasoning* with some rational underpinning to support the legal conclusion of obviousness.” *KSR Int’l v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (emphasis added)).

In the Final Office Action of February 4, 2010, the Examiner asserted that the combination of Hiramoto and Hutter discloses all elements of claim 1. However, the Examiner failed to even address that claim 1 requires that the first and second guard rings extend through a buried insulation layer contacting a semiconductor substrate as required by claim 1. In fact, the Final Office Action was silent on any discussion whatsoever of this claim language.

In response to the Final Office Action, Applicant submitted an Amendment After Final on March 24, 2010. In the Amendment, Applicant pointed out the above-mentioned deficiency of the Final Office Action, i.e., that the Examiner did not address the requirement of claim 1 that the first guard ring and second guard ring extends through a buried insulation layer contacting a semiconductor substrate. The Examiner issued an Advisory Action on April 7, 2010, in which the Examiner stated the following:

Applicant argues that the limitation “that the first and second guard ring extend through a buried insulation layer contacting a semiconductor substrate” since the rejection does not expressly use such claim language. As a preliminary matter examiner notes that a rejection is not a mere regurgitation of claim language but rather a technical understanding of why the limitations of a claim are met by the prior art. In other words, the claims describe the invention they are not the invention unto themselves.

Applicant respectfully submits that the above statements, which are apparently directed to the legal requirements for establishment of a *prima facie* case of obviousness, do not bridge the gap between the teachings of the applied references and the limitations recited in Applicant’s claims. As mentioned above, a *prima facie* case of obviousness requires support for all elements of the rejected claim. In the above statements from the Advisory Action, however, the Examiner

appears to assert that, although the missing language of claim 1 was not addressed in the rejection of claim 1, the Examiner's burden has still been satisfied. However, the Final Office Action still did not include any acknowledgement, via exact claim language or otherwise, of these elements of claim 1. Simply put, the outstanding grounds of rejection fail to address an explicit requirement of Applicant's claims. As such, the Examiner clearly did not set forth a prima facie case of obviousness.

In response to Applicant's argument that a prima facie case has not been established, the Examiner further stated:

In the instant case Hiramoto's discloses guard rings contacting a buried oxide, and the deficiency of contacting the substrate is cured by Hutter. One of ordinary skill in the art would clearly recognize that this modification would result in the guard rings extending through the buried oxide to reach the substrate

Hutter is directed to a bulk semiconductor device that does not include a buried insulator layer as claim 1 requires. Hutter merely describes that a trench is "etched downwardly through the mask opening... into the underlying substrate." Hutter at column 2, lines 32-37. Similarly, Hiramoto discloses a separating groove that is formed in a portion of a semiconductor substrate above a buried oxide layer in the substrate. Indeed, Hiramoto describes the upper portion of an SOI substrate (portion above the insulator), as the substrate. "In Japanese Patent Laid-Open No. 184068/1990, there is disclosed a process of forming an n-type well region and a p-type well region over a silicon substrate (i.e., Silicon On Insulator substrate, as will be shortly referred to as the "SOI substrate") formed over an insulating layer..." Hiramoto at column 1, line 66-column 2, line 3.

Hiramoto and Hutter disclose forming a trench (Hutter), or forming separating groove (Hiramoto), that contacts a substrate. Thus, the Examiner's proposal to modify the Hiramoto device by the teachings of Hutter would not result in any change at all to the Hiramoto device, since the Hiramoto separating groove already contacts the device substrate (the substrate above the buried oxide layer) as taught by Hutter. The Hiramoto separating groove, since it already contacts the substrate, would still extend to the buried oxide layer as explicitly stated in Hiramoto. Hiramoto Abstract and at column 7, lines 19-29. Thus, even if Hiramoto were modified per Hutter, as suggested by the Examiner, the resulting combination would not even result in the requirements of claim 1.

Furthermore, in the Advisory Action, the Examiner did not identify any apparent reason why one of ordinary skill in the art would have undertaken the modification of the Hiramoto integrated circuit in view of the Hutter integrated circuit. Instead, the Examiner merely concluded that "the deficiency of contacting the substrate is cured by Hutter," without any articulated reasoning as to why the Examiner came to this conclusion. The Examiner further stated that "[o]ne of ordinary skill in the art would clearly recognize that this modification would result in the guard rings extending through the buried oxide layer," without any explanation as to why one of skill in the art would recognize this modification. Applicant respectfully submits that the disputed element of claim 1 is not that the guard rings contact the substrate. The disputed element of claim 1 is that the first guard ring and second guard ring extends through a buried insulation layer. Therefore, Applicant respectfully submits that the above statements cannot be considered articulated reasoning with some rational underpinning to support all elements of claim 1, as required to support a prima facie case of obviousness. The Examiner has clearly erred in his rejection of claim 1, and therefore claim 1 should be placed in condition for allowance.

CONCLUSION

For at least the reasons stated above, the rejection of at least independent claim 1 was improper and must be reversed. Applicant requests a review and a panel decision that promptly resolves the issues in Applicant's favor and eliminates the need for an Appeal Brief.

Please charge any additional fees or credit any overpayment to Deposit Account Number 50-1778. The Examiner is invited to telephone the below-signed attorney to discuss this application.

Date:

May 4, 2010

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